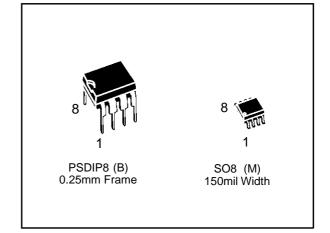


ST95040 ST95041

SERIAL ACCESS SPI BUS 4K (512 x 8) EEPROM

DATA BRIEFING

- 100,000 ERASE/WRITE CYCLES
- 40 YEARS DATA RETENTION
- SINGLE 4.5V to 5.5V SUPPLY VOLTAGE
- SPI BUS COMPATIBLE SERIAL INTERFACE
- 2 MHz CLOCK RATE MAX
- BLOCK WRITE PROTECTION
- STATUS REGISTER
- 16 BYTE PAGE MODE
- WRITE PROTECT
- SELF-TIMED PROGRAMMING CYCLE
- E.S.D.PROTECTION GREATER than 4000V
 SUPPORTS POSITIVE CLOCK SPI MODES
- (ST95040) SUPPORTS NEGATIVE CLOCK SPI MODES
- SUPPORTS NEGATIVE CLOCK SPI MODES (ST95041)



Logic Diagram

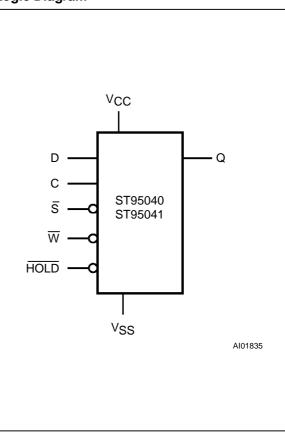
DESCRIPTION

The ST95040 and ST95041 are 4K bit Electrically Erasable Programmable Memories (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. The memory is accessed by a simple SPI bus compatible serial interface. The bus signals are a serial clock input (C), a serial data input (D) and a serial data output (Q).

The device connected to the bus is selected when the chip select input (\overline{S}) goes low. Communications with the chip can be interrupted with a hold input (HOLD). The write operation is disabled by a write protect input (\overline{W}) .

For the ST95040, data is clocked in during the low to high transition of clock C, data is clocked out during the high to low transition of clock C.

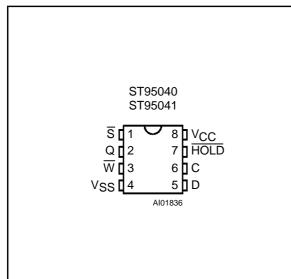
For the ST95041, data is clocked in during the high to low transition of clock C, data is clocked out during the low to high transition of clock C.



B95040/606

Complete data available on DATA-on-DISC CD-ROM or at www.st.com

DIP Pin Connections

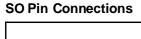


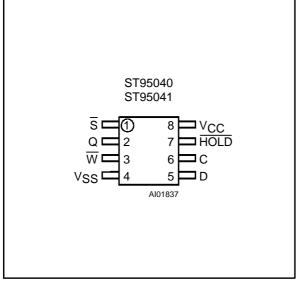
Signal Names

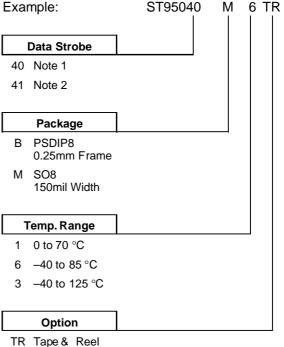
С	Serial Clock
D	Serial Data Input
Q	Serial Data Output
s	Chip Select
W	Write Protect
HOLD	Hold
Vcc	Supply Voltage
V _{SS}	Ground

Ordering Information Scheme For a list of available options refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.







Packing

- Notes: 1. Data In is strobed on rising edge of the clock (C) and Data Out is synchronized from the falling edge of the clock.
 - 2. Data In is strobed on falling edge of the clock (C) and Data Out is synchronized from the rising edge of the clock.

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